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Multifunctional Half-Floating-Gate Field-Effect Transistor Based on MoS_2−BN−Graphene van der Waals Heterostructures

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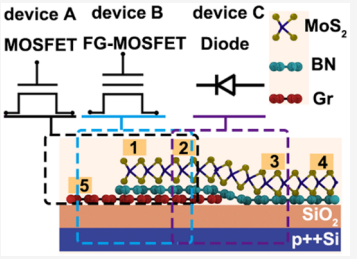
ABSTRACT: Multifunctional electronic devices that combine logic operation and data storage functions are of great importance in developing next-generation computation. The recent development of van der Waals (vdW) heterostructures based on various two-dimensional (2D) materials have brought exceptional opportunities in designing novel electronic devices. Although various 2D-heterostructure-based electronic devices have been reported, multifunctional devices that can combine logic operations and data storage functions are still quite rare. In this work, we design and fabricate a half-floating-gate field-effect transistor based on MoS_2−BN−graphene vdW heterostuctures, which can be used for logic operations as a MOSFET, nonvolatile memory as a floating-gate MOSFET (FG-MOSFET), and rectification as a diode. These results could lay the foundation for various applications based on 2D vdW heterostuctures and inspire the design of next-generation computation beyond the von Neumann architecture.



KEYWORDS: *heterostructures, half-floating gate, multifunction, nonvolatile memory, diode*

The current fast-developing information technology has imposed an urgent need for high-performance and energy-efficient computation. However, the traditional von Neumann architecture with separate data processing and storage parts has limited the performance and energy efficiency of conventional computers.[1] Developing next-generation computation beyond the von Neumann architecture has attracted intense interest among scientists and engineers.[2−4] Among those efforts, designing new electronic devices combining both logic operation and data storage functions as the basic building block for microchips is a promising approach and the key challenge of this approach is to find appropriate materials suitable for the new device design.[5]

In recent years, the rise of two-dimensional (2D) materials has brought new opportunities for electronic device designs.[6] Two-dimensional materials possess various electronic properties, including good insulators such as hexagonal boron nitride (h-BN), semimetals such as graphene, and semiconductors such as molybdenum disulfide (MoS_2).[7] The flat 2D geometry and atomically thin structure are compatible with present silicon processing technologies. Furthermore, different 2D materials can be vertically assembled to form van der Waals (vdW) heterostructures through weak vdW interactions, without being constrained by a lattice mismatch, which can combine different properties of various 2D materials and bring exceptional flexibility to device designs.[8] Up to now, a range of 2D vdW heterostructure based devices have been demonstrated, such as graphene/hexagonal boron nitride resonant tunneling diodes,[9,10] the tunneling transistor made from black phosphorus (BP)/Al_2O_3/BP,[11] and multijunction lateral heterostructures based on $MoSe_2/WSe_2$.[12] However, few results have been reported regarding multifunctional devices that can combine logic operations and data storage functions.

We report a half-floating-gate (HFG)-controlled field-effect transistor (FET) based on graphene, h-BN, and MoS_2 vdW heterostructures. We indicate that three different functions, including MOSFET, floating-gate MOSFET (FG-MOSFET), and a diode, can be achieved and modulated in a single device. The obtained devices show excellent and unique properties and could pave the way for diverse applications in electronics and optoelectronics, such as nonvolatile memories, rectifiers, photovoltaics, and photodetectors. This device shows on/off ratios of 10^5 as a logic MOSFET, rectification ratios of 10^3 as a diode, and 10-year retention as an FG-MOSFET, respectively. In addition, combining logic operation and data storage functions in an individual transistor might facilitate the design of next-generation computation beyond the von Neumann architecture.

Figure 1a describes the device structure of the MoS_2−h-BN−graphene-based half-floating-gate field-effect transistor (HFG-FET) device. MoS_2 serves as the channel material, while hexagonal boron nitride (h-BN) and graphene act as the tunneling layer and floating gate, respectively. Only half of the region of the MoS_2 flake is aligned over the graphene film to produce a HFG-FET device structure. The fabrication process

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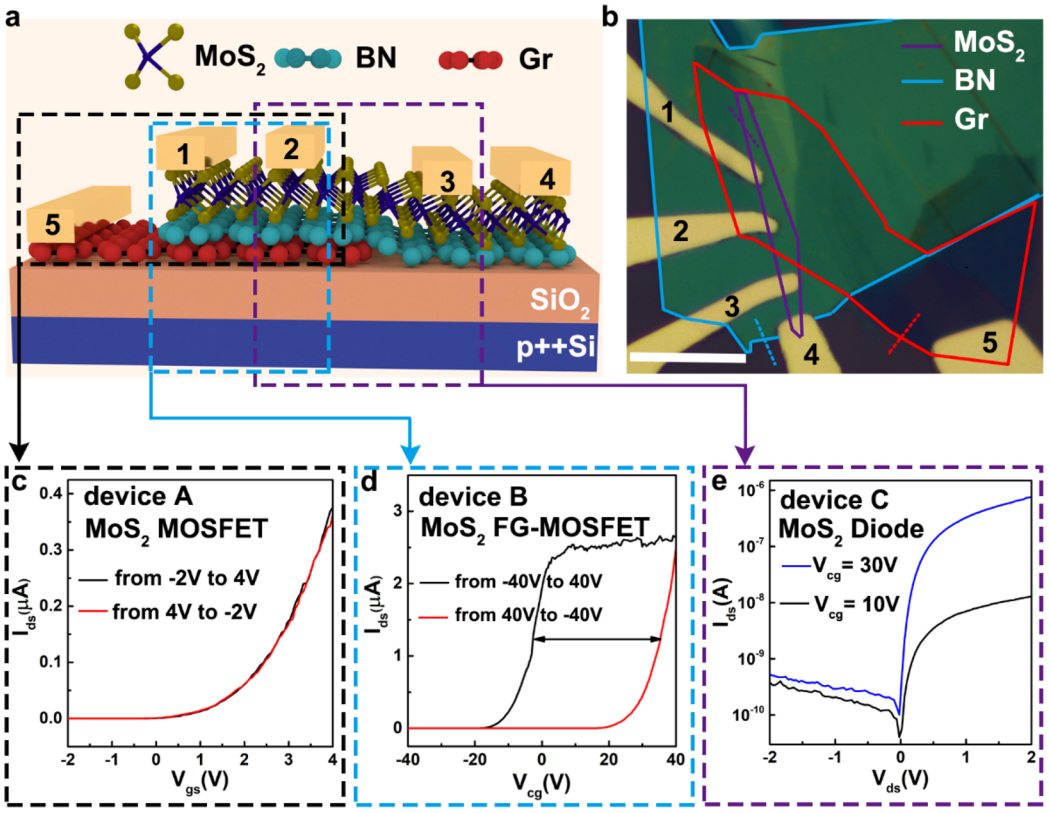

Figure 1. MoS_2−h-BN−graphene vdW heterostructures for HFG-FET. (a) Diagram of MoS_2−h-BN−graphene HFG-FET. MoS_2 is the channel, graphene is the HFG, h-BN is the tunneling layer, and a p-type Si substrate is the control gate. (b) Optical image of a typical fabricated device. The regions of MoS_2, h-BN, and graphene in heterostructures are marked by solid lines in violet, blue, and red, respectively. The scale bar is 20 μm. Thickness profiles of MoS_2, h-BN, and graphene characterized at the regions tagged by dashed lines in violet, blue, and red in (a), respectively. (c) I_{ds}−V_{gs} curve of the MoS_2 MOSFET in the device. There were no obvious threshold voltage shifts when V_{gs} was swept back and forth from −2 to +4 V. Electrodes 1, 2, and 5 are the source, drain, and gate in MOSFET, respectively, (d) I_{ds}−V_{cg} curves of the MoS_2 FG-MOSFET in the device. There is a threshold voltage shift when V_{cg} is swept back and forth from −40 to +40 V. Electrodes 1 and 2 and Si are the source, drain, and control gate in FG-MOSFET, respectively. (e) I_{ds}−V_{ds} curves of the MoS_2 diode in the device under different values of control gate voltage. Electrodes 2 and 3 are the cathode and anode in the diode, respectively.

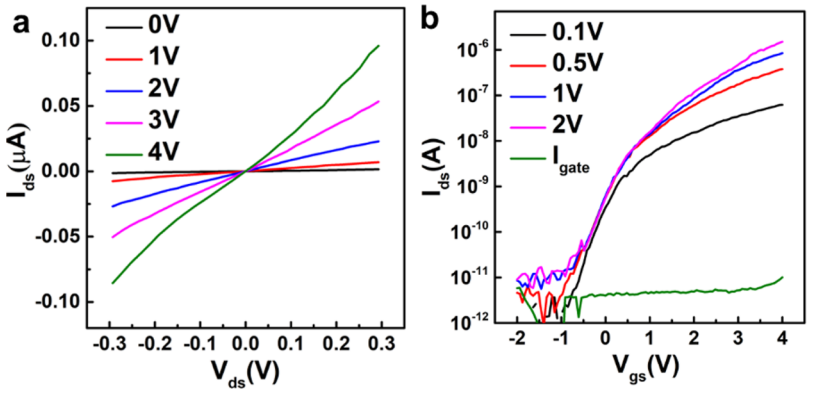

Figure 2. Characterization of MOSFET in MoS_2−h-BN−graphene vdW heterostructures for HFG-FET. (a) I_{ds}−V_{ds} curves under different values of V_{gs}. The linear dependence of of I_{ds}−V_{ds} shows that the contacts are Ohmic. (b) I_{ds}−V_{gs} curves under different values of V_{ds}. The green line is the gate leakage current (I_g) under a bias voltage with 2 V.

is illustrated in Figure S1. Figure 1b presents an optical micrograph of a representative MoS_2−h-BN−graphene heterostructure. The 2D heterostructures were first characterized by Raman spectroscopy and atomic force microscopy (AFM)[13−17] (see Figures S2 and S3, respectively, for more details). In this 2D van der Waals heterostructure based HFG-FET device, one MOSFET, one floating-gate MOSFET, and one diode are integrated into a single device (see Figure 1a). The MOSFET (device A) is marked by the black dashed rectangle in Figure 1a, where MoS_2, h-BN, and graphene flakes form the device channel, dielectric material, and gate, respectively. Electrodes 1 and 2 form the source and drain, and electrode 5 functions as the gate electrode. The floating-gate MOSFET (device B) is marked by the blue dashed rectangle in in Figure 1a, where a p-type Si substrate serves as a control gate electrode, while MoS_2, h-BN, and graphene are

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Nano Lett. XXXX, XXX, XXX−XXX

used as the channel, tunneling, and trapping layer, respectively. In this case, electrodes 1 and 2 still function as source and drain electrodes. The diode (device C) is marked by violet dashed rectangle in Figure 1a. In this device, only half of the region of the MoS_2 is aligned over the graphene to form a half-floating-gate device architecture, where MoS_2 serves as the transport channel, graphene is the half-floating gate and the p-type Si substrate is the control gate. Electrodes 2 and 3 function as source and drain electrodes. Figure 1c–e shows the circuit element symbols and characteristic electronic properties of the integrated MOSFET, FG-MOSFET, and diode devices, respectively. The detailed electronic characterizations and working mechanisms of these devices will be discussed in detail in the following.

We first studied the electronic characteristics of the MOSFET (device A). We applied a voltage V_{gs} to the graphene flake, separated from MoS_2 by the 30 nm thick h-BN flake. Figure 2a shows the $I_{ds}-V_{ds}$ characteristic of device A. The linear dependence of $I_{ds}-V_{ds}$ indicates good Ohmic contacts between the MoS_2 flake and metal electrodes. From the transfer characteristics presented in Figure 2b, we can calculate the low-field field-effect electron mobility of 15 $cm^2 V^{-1}s^{-1}$ using eq 1[18]

$$\mu = \frac{dI_{ds}}{dV_g} \times \frac{L}{WC_iV_{ds}} \quad (1)$$

where L = 5.5 μm is the channel length, W = 1.6 μm is the channel width, and $C_i = 1.03 \times 10^{-3}$ F/m^2 is the capacitance between the channel and the back gate per unit area. Note that this value indicates the lowest limit of electron mobility because contact resistance is ignored. The green line in Figure 2b is the gate leakage current (I_g), which is 1 order of magnitude lower than I_{ds} at the off state and 5 orders of magnitude smaller at the on state. This means that the 30 nm thick h-BN layer has excellent electric insulating properties. This device shows an electron mobility of 15 cm^2 V^{-1} s^{-1}, current on/off ratios of 10^5, and an on-state current density of 0.25 μA/μm under a drain-source bias (V_{ds}) at +2 V, which are of the same order of magnitude as in previous studies.[19]

Then we studied the electronic properties of the floating-gate MOSFET (device B). The working mechanism of this 2D-heterostructure-based memory is represented in Figure 3. Figure 3a shows the flat energy band diagram of the MoS_2–h-BN–graphene heterostructures. The work function of few-layer graphene is 4.6 eV.[20] The electron affinity of few-layer MoS_2 is about 4.0 eV. Its band gap varies from 1.2 to 1.8 eV, which is decided by the number of layers.[21,22] As a dielectric layer, h-BN has a relatively small electron affinity (2.0–2.3 eV) and a large band gap (5.2–5.9 eV).[23] It can produce large potential barriers for electrons between graphene and MoS_2. As presented in Figure 3b, when a positive voltage is applied on the Si substrate, electrons are accumulated in the MoS_2. Simultaneously, a large positive electrical potential is built between the graphene and MoS_2, which forces the accumulated electrons to tunnel from the MoS_2 to the floating-gate graphene (see Figure 3b,c). Once the positive voltage is removed from the Si substrate (see Figure 3d), the electrons in the channel will disappear. In contrast, the tunneled electrons are still trapped in the graphene due to the large potential barriers of the h-BN and SiO_2. No electrons could pass through the source to the drain, and the device is switched to the off state. This is the programming process for the FG-MOSFET. Correspondingly, electrons will be extracted from the half floating gate when a negative gate voltage is applied on the Si substrate (see Figure 3e,f). The carrier's concentration in the MoS_2 will be set back to the original baseline level (see Figure 3g), and the device is switched to the on state. This is the erasing process for the FG-MOSFET.

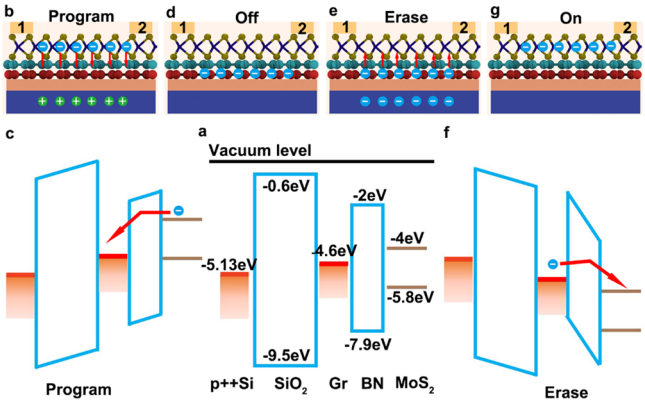

Figure 3. Working mechanisms of this 2D-heterostructure-based floating-gate FG-MOSFET explained by simplified band diagrams. (a) Energy band diagrams of different materials comprising the heterostructures before being brought into contact. E_C and E_V are the positions of the bottom of the conduction band and the top of the valence band, respectively. (b) Charge-doping state of the device with a positive gate voltage. (c) Flat energy band diagram when a positive gate voltage is applied. (d) Charge-doping state of the device after the positive gate voltage is removed. (e) Electron extraction from the graphene when a negative gate voltage applied. (f) Flat energy band diagram when a negative voltage is applied. (g) Charge-doping state of device after the negative gate voltage is removed.

We measured the transfer characteristic of device B, and the results are shown in Figure 4a. The memory characteristics demonstrate themselves in a threshold voltage (V_{th}) shift dependent on the amount of charge trapped in the graphene layer. The hysteresis of the transfer curves defines a memory window of ~35 V. Here, we can use eq 2 to estimate the density of the charges stored in the graphene floating gate

$$n = \frac{\Delta V \times C_{cg\text{-}fg}}{q} \quad (2)$$

where q is the electron charge and ΔV is the threshold voltage shift (35 V here for the scanning range of −40 to +40 V). $C_{cg\text{-}fg}$ is the capacitance between the Si control gate and graphene floating gate, calculated by eqs 3 and 4:[24]

$$\frac{1}{C_{cg\text{-}fg}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{BN}} + \frac{1}{C_{graphene}} \quad (3)$$

$$C = \frac{\varepsilon_0\varepsilon_r}{d} \quad (4)$$

The ε_r values for SiO_2, graphene, and h-BN are 3.9, 5.6, and 3.5, respectively.[25,26] We can determine that the density of the stored charges is about 2.2×10^{12} cm^2.

The drain-source current (I_{ds}) versus V_{ds} was measured when a constant V_{cg} was applied to the gate (as shown in Figure 4b). The memory state of device B could be read out via measuring I_{ds} at a constant V_{ds}. The results show that the ON and OFF states of memory device B could be switched with V_{cg}. At the ON state, the linear behavior of $I_{ds}-V_{ds}$ indicates Ohmic-like contacts between the device channel and

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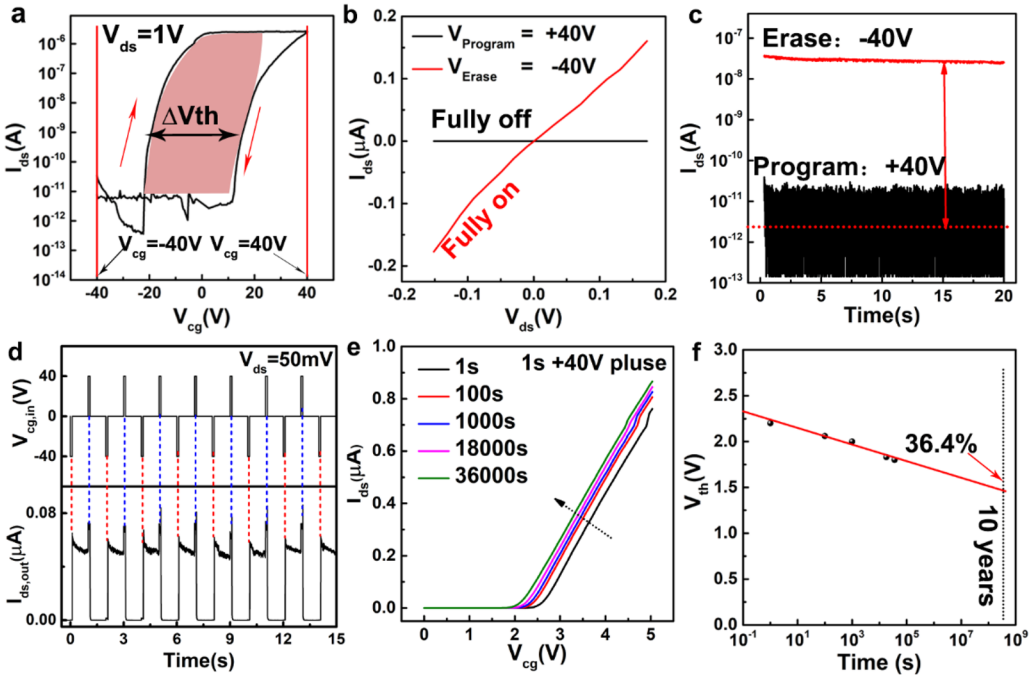

Figure 4. Characterization of nonvolatile memories in MoS_2−h-BN−graphene vdW heterostructures for HFG-FET. (a) I_{ds}−V_{cg} of the HFG-FET when V_{cg} is swept back and forth from −40 to +40 V. The memory window of this device is estimated to be 35 V. (b) I_{ds}−V_{ds} of the HFG-FET in the ON and OFF states. (c) Retention characteristics of the HFG-FET at the programmed/erased states. These two different states were measured at V_{cg} = 0 V and V_{ds} = +50 mV after a programming/erasing pulse voltage was applied (+40 V/−40 V, 100 ms). (d) Dynamic switching behavior between ON and OFF states produced by applying a periodic programming/erasing pulse (+40 V/−40 V, 100 ms). (e) I_{ds}−V_{cg} obtained at different time intervals. The pulse was +40 V, and the duration time was 1 s. (f) Time-resolved evolution of V_{th} after a programming pulse was applied.

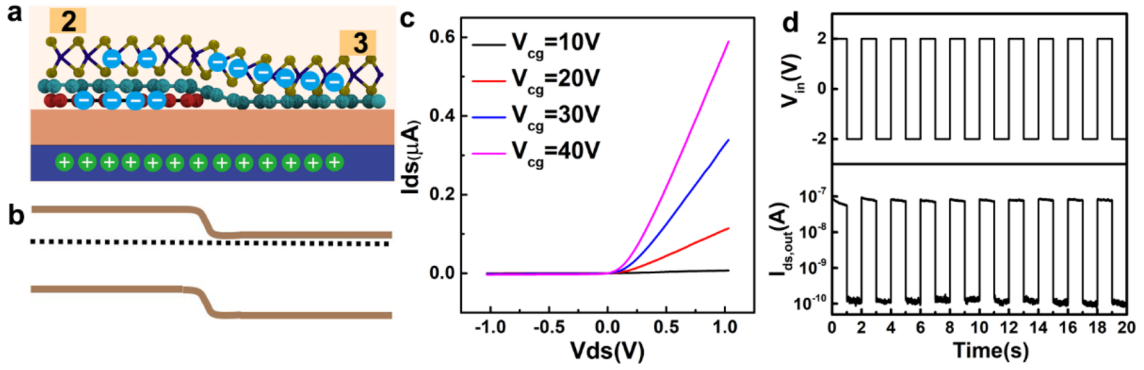

Figure 5. Characterization of diode in MoS_2−h-BN−graphene vdW heterostructures for HFG-FET. (a) Charge-doping state of the heterostructure (b) Energy band diagram along the MoS_2 n^+−n junction. (c) I_{ds}−V_{ds} curves across the MoS_2 with different gate voltages. (d) Dynamic I_{out}−V_{in} curve obtained by sweeping V_{in} from −2 to +2 V.

the metal electrodes. The retention ability of the programming/erasing state of device B was also studied because it is vital for data storage. As depicted in Figure 4c, device B was programmed (erased) through a +40 V (−40 V) voltage pulse (100 ms). An on−off current ratio of over 10^3 was maintained during the consistent testing of 20 s. The on-state current presented a small change, while the off-state current varied from 10^{-13} to 10^{-11} A. Significantly, these results illustrate that the memory device B has reliable retention ability. As shown in Figure 4d, we further investigated the dynamic switching characteristics of device B between two different states. Flipping between the programmed and erased states was controlled under a ±40 V 100 ms pulsed signal applied to the control gate, while the V_{ds} value was set at +50 mV. Originally, device B remained in a low-current state, corresponding to the OFF (programmed) state. As a negative voltage pulse (−40 V, 100 ms) was applied, device B was rapidly converted into the ON (erased) state, holding a stable high current of ∼0.06 μA. When the pulsed signal was removed, the device still worked in the ON state. Device B was restored to the initial OFF state (10^{-11} A) after applying a symmetric positive pulse (+40 V, 100 ms) on the control gate. Here we use a traditional method for memories to estimate the retention of the trapped charges in device B. The threshold voltages are dependent on the trapped charges in the device. This means that we can estimate the trapped charges' retention on the basis of the variation of the threshold voltage. In Figure 4e, the transfer curves were achieved by sweeping V_{cg} within a relatively small range from 0 to +5 V, which can effectively avoid undesirable carrier depletion/injection at the graphene floating gate. As shown in

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Nano Lett. XXXX, XXX, XXX−XXX

Figure 4f, the extracted threshold voltage decreased from 2.2 to 1.8 V after 10^4 s, almost exponentially dependent on the time. We can thus estimate that 36.4% of the trapped charges would disappear after 10 years. Therefore, we consider that device has a 10-year retention because the charge leakage from the floating gate is rather slow. This result fully explains that device B in the heterostructures is a promising candidate for nonvolatile memory applications.

Finally, we studied the rectification behavior of the diode device (device C). The working mechanism of device C is very similar to the half-floating-gate-controlled programmable p−n junction reported by Li et al. in a previous study.[27] The Si control gate is manipulated to control the amount of electrons trapped in the graphene flake and introduce a potential barrier between the right part of the MoS_2 channel and the left part overlapped with graphene. As shown in Figure 5a, a positive voltage made electrons accumulate in the channel due to the field effect. Meanwhile, a positive electrical potential will induce these electrons to tunnel from the MoS_2 to graphene. The large potential barriers of the h-BN and SiO_2 can effectively trap these electrons in the graphene layer. These trapped electrons can screen the positive potential of the control gate and reduce the charge concentration in the left part of MoS_2 overlapped with the graphene layer. In the previous work reported by Li et al., the authors used ambipolar 2D WSe_2 as the device channel and the left part of WSe_2 can be modulated to be p-type doped after programming with a positive gate voltage; thus, a programmable p−n junction can be achieved. In our case, 2D MoS_2 shows unipolar characteristics (see Figure 3b). Due to the Fermi level pinning effect, the left part of MoS_2 is still n-type doped after programming, but the charge carrier concentration was reduced dramatically. In this way, a n^+−n junction is created along the MoS_2 channel. Figure 5b shows the possible band structure of the created n^+−n junction with the MoS_2 bent over the edge of the graphene. Figure 5c shows the I_{ds}−V_{ds} curve with a control gate voltage of +10−40 V. It shows an evidently rectifying behavior with a rectification ratioof over 10^3 (at $V_{ds} = \pm 2$ V). The electrical transport across the n^+−n diodes can be expressed by the modified Shockley equation (5)

$$I_{ds} = \frac{nV_T}{R_S} W\left[\frac{I_0 R_S}{nV_T} \exp\left(\frac{V_{ds} + I_0 R_S}{nV_T}\right)\right] - I_0 \quad (5)$$

where $V_T = k_B T/e$ is the thermal voltage at temperature T. k_B, e, I_0, W, and n are the Boltzmann constant, electron charge, reverse saturation current, Lambert W function, and ideality factor, respectively.[28,29] R_S is the series resistance. By fitting the I_{ds}−V_{ds} curves with this transport model, we find that the n^+−n junction has $n = 1.45$, $I_0 = 4 \times 10^{-10}$ A, and $R_S = 1.1$ MΩ, which can be modulated further by varying the voltage (as shown in Figure S4). The value of the ideality factor usually shows the transport mechanism of the diode. If $n = 1$, the diffusion mechanism will play an important role in diodes. When $n = 2$, the mechanism is controlled by a recombination process. The large ideality factors (1.45−1.75) of the diode in HFG-FET explain that the transport is controlled by the recombination process. A large density of the trap states often exists on the MoS_2 surface because of nonideal processes for material growth and device fabrication. These trap states could serve as the recombination centers.[30] In comparison with the I_{ds}−V_{ds} curves of device B in Figure 2a and device D (electrodes 3 and 4 as source and drain, respectively) in Figure S5, the linear behavior of I_{ds}−V_{ds} curves of MoS_2 devices without an HFG structure exhibit no rectification characteristics. Figure 5d further presents the dynamic performances of the n^+−n junctions with a reverse $V_{ds} = -2$ V and a forward $V_{ds} = +2$ V (+40 V applied on the Si control gate). The result exhibits that the device can be switched well between the the ON and OFF states by applying different voltages.

In conclusion, we designed and fabricated a multifunctional half-floating-gate (HFG)-controlled field-effect transistor based on van der Waals integrated MoS_2−h-BN−graphene heterostructures. MOSFET, floating-gate MOSFET, and diode functions were successfully achieved in this single device configuration simultaneously. As a classical MOSFET, this device can be used for logic operation. As an FG-MOSFET, it can be retained for 10 years with an on/off ratio of 10^3. As a n^+−n diode, it exhibits good rectifying characteristics with a rectification ratio of up to 10^3 and this value can be further modulated by different V_{cg} values. Our multifunctional HFG-FET could find potential applications in logic operations, data storage, rectifier switching, etc. Moreover, a single device that combines logic operation and data storage functions might pave the way for designing next-generation computation beyond the von Neumann architecture.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c04737.

More details of the experimental methods, Raman spectra of the MoS_2−h-BN−graphene heterostructure, AFM images of the MoS_2−h-BN−graphene heterostructure, semilogarithmic plots of I_{ds} through the MoS_2 n^+−n diodes, and I_{ds}−V_{ds} curves recorded for different values of V_{gs} of the MoS_2 MOSFET (PDF)

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Nano Lett. XXXX, XXX, XXX−XXX

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Notes

The authors declare no competing financial interest.

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